Iker Garcia Morales

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Electrical Engineering and Robotics student focused on VLSI, RTL design, hardware verification, and CPU architecture. Founder and lead developer of Simple Silicon, a desktop EDA environment for SystemVerilog design, simulation, waveform inspection, and RTL visualization.

SKILLS:

Hardware Description Languages: SystemVerilog, Verilog, VHDL
Programming: Python, C/C++, MATLAB.
Processor & Digital Design: ISA Design, RTL Design, Multicycle Datapaths, FSMs, Digital Logic
VLSI & ASIC Design: CMOS Schematic and Layout, DRC, ERC, NCC, ASIC Design Flow
Simulation & Tools: Electric VLSI, ModelSim, Quartus Prime, Yosys, Git, LTspice, Linux
Embedded Systems: Arduino, ESP32, STM32.

EDUCATION:

John Brown University, Siloam Springs, AR
B.S. in Electrical Engineering; Double Major in Robotics and Mechatronics Engineering
Expected May 2027
Relevant Coursework
Digital IC Design, Digital Electronics, Embedded Systems, Electronics, Electrical Circuits, Control Systems.

PROJECTS:

Simple Silicon — Founder & Lead Developer (TypeScript, React, Rust/Tauri, Yosys)

Developing a desktop EDA environment for SystemVerilog design, integrating RTL editing, simulation, waveform inspection, and interactive hardware visualization. Built an RTL Visualizer that uses Yosys to elaborate designs and display module hierarchy, internal logic, gates, multiplexers, signals, and connections. Designed the product architecture, interface, and verification workflows with a focus on making digital hardware development more accessible and intuitive.

Silicio-16: Custom 16-bit Processor (SystemVerilog)

Designed and verified a custom 16-bit multicycle processor in SystemVerilog featuring eight general-purpose registers, a 16-instruction ISA, and support for arithmetic, logic, memory, comparison, branch, and jump operations. Implemented the complete datapath and FSM-based control unit and validated full-program execution using a self-checking regression suite.

ASIC Design: 8-bit MIPS Processor (Electric VLSI)

Designed an 8-bit MIPS-style processor using a bit-slice architecture, including the datapath, ALU, register structures, and FSM-based control unit. Completed full-custom CMOS schematic and layout, passed DRC, ERC, and NCC verification, simulated the processor using IRSIM, and integrated the core into a MOSIS TinyChip padframe.

Content-Addressable Memory (SystemVerilog)

Implemented a synthesizable 4-entry, 32-bit CAM with synchronous writes, valid-bit tracking, parallel combinational lookup, and match/miss outputs. Developed a self-checking testbench that passed all 10 functional tests.

EXPERIENCE:

John Brown University — Siloam Springs, AR
Teaching Assistant – Digital Electronics
Jan 2025 – May 2026
Facilitate digital circuit design and troubleshooting labs, support students working with logic gates, flip-flops, multiplexers, and counters, and evaluate assignments for circuit correctness and technical precision.
Learning Coach and Engineering Tutor – Student Support Services
Sep 2024 – Present
Provide one-on-one and small-group support in calculus, electrical circuits, technical problem-solving, and study strategies for engineering students.

LEADERSHIP & AWARDS

IEEE Student Branch – Junior Senator
Student Government Association – Freshman Senator, Junior Senator.
Walton International Scholarship Scholar.